EE432 Advanced Digital Design with HDL
Spring 2013
Course Overview
Instructor: Tom Almy

Objectives

The student will be able to design digital systems using VHDL that incorporate multiple state machines and asynchronous as well as synchronous signals. The student will be able to write simulation test benches to verify operation both functionally and with timing constraints. The student will be able to use synthesis macros (Xilinx Core Generators). The student will be able to realize the designs in FPGAs and demonstrate operation.

Class Meetings

We will meet Tuesday evenings, April 2 through June 11, 5:30 to 9:50 PM. All assignments must be turned in by June 11 at 5:30 PM. There will be no final exam. The team projects will be demonstrated on June 11.

Instructor Access

Send email to xxxxx. My home phone is xxxxxxxxxx, and I am available evenings and on the weekends (before 9PM, please). However email is usually better.

I typically arrive between 4 and 4:30 on class nights and am available for questions until the start of classes at 5:30.

There is also a forum I have set up at xxxxxxxxxx. Set up an account and post there. Also check this site regularly for class information.

I send out important information via email to all students. I use your OIT address unless you have given me an alternative.

Cell Phones

Please turn off cell phones or make them "silent" during class to avoid disturbing the class.

Required Textbook and Hardware

The Nexys-3 FPGA board will be needed. Order from http://www.digilentinc.com. Some team members can use the older Nexys-2 but final integration will require a Nexys-3. The Nexys-2 cannot be used for the memory system or UART designs. There will be a DVD containing software and documentation for the course that will be provided the first session if you don't already have it from EE331. Most lab work can be done at home or elsewhere with a computer that has 8-9 GB free disk space, 1 GB RAM, an available USB port, and Internet access. Windows XP through Windows 7 is required. The software currently does not work on Windows 8 systems (as far as I know). The final project will require either a computer with two USB ports (and two cables to connect to the Nexys-3 board) or two computers each with a USB port and a cable to connect to the Nexys-3 board.

There are no textbook assignments. You may use your Pedroni or Roth textbook from an earlier course for reference. Other important references are provided on the DVD or in the ZIP file handout.

The Course Project

In order to get the best learning experience in digital systems, the bulk of the course effort will be in a single project done by the entire class, with each student assigned a portion of the design. See the document ProjectOverview.pdf for a full description. Each student is to keep a dated journal of their work on the project. The journal is to be maintained in a single document file. The journal is to be submitted each week to xxxxxxxxx.

The complete VHDL and PDP-8 assembly language listings for the projects must be turned in June 11 by the team.

Reading and Homework Assignments

An assignment sheet for each week lists the lecture topics, reading which should be completed prior to class, and the homework assignment due the following week. The assignment sheets are in the ZIP file and are labeled by week number.

There are a limited number of homework assignments and the subject matter will be of general usefulness in completing the course project.

The homework assignments are due at 5:30 PM on the evening of the class. Assignments should be turned in via email. Send homework assignments to xxxxxxxxx. There is a 20% penalty for homework assignments turned in up to a week late. There is no Virtual Late Card for this course.

The homework assignments typically require using the Xilinx ISE and writing VHDL. In most case (unless otherwise instructed) turn in your VHDL code for your answer. This should be either a single VHDL file (if applicable) or a ZIP file containing all the VHDL files. BE SURE YOUR NAME IS IN ALL THE VHDL FILES! The ZIP file should

have a name that includes your name and the assignment so that all the ZIP files will be unique. For instance, my first homework assignment ZIP file would be named *almy_hwk1.zip*.

Grading

Grading is weighed as follows:

Component	Worth	Total
Homework Assignment	7%	35%
Lecture Evaluation Forms	0.5%	4%
Weekly Journal	1 2/9%	11%
Week 6 project deliverables	5%	5%
Week 8 project deliverables	10%	10%
Project Completion	35%	35%

Note that if your team successfully demonstrates your PDP-8 on June 11, everyone on your team gets full credit on all three project items (the week 6 and 8 deliverables and project completion). There is no partial credit for the week 6 and 8 project deliverables, however there is partial credit available for "Project Completion" in the case the demonstration is not successful. The grading scale is 90-100 A, 80-<90 B, 70-<80 C, 60-<70 D, <60 F.

EE432 Spring 2013 Schedule

Date	Week	Lecture Subject	Assignment Due
Apr 2, 2013	1	Project	
Apr 9, 2013	2	State Machines (and the project)	Homework 1
Apr 16, 2013	3	Synchronization and State Machines	Homework 2
Apr 23, 2013	4	Xilinx FPGA Structure and COREGEN	Homework 3
Apr 30, 2013	5	FPGA Interfacing	None
May 7, 2013	6	Clocks and Timing	Week 6 project deliverables
May 14, 2013	7	FPGA Project Organization	Homework 4
May 21, 2013	8	DDR and Tristate	Week 8 project deliverables
May 28, 2013	9	Project Issues	Homework 5
Jun 4, 2013	10	Project Issues	None
Jun 11, 2013			Demonstration of PDP-8!

Updated Journal is due every week — April 9 through June 4 (9 total).
Project issues will also be discussed as needed during the early weeks of the term.