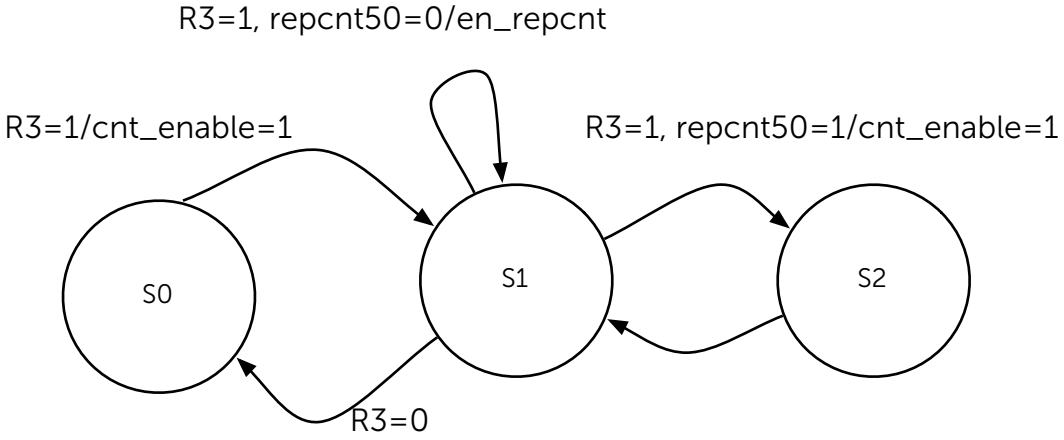
EE 331 Digital Systems with HDL
Oregon Tech, Wilsonville, Winter 2014

Lab Assignment 4, due Week 6, February 11

In this lab you will modify the lab 3 design so that as long as the button stays depressed the counter will increment every 500 ms. You are to do this by replacing the one-shot (which will only allow the counter to increment once per button depression) with a state machine You will also need an additional counter that when enabled increments every 10 ms (you already have a signal that produces a pulse every 10 ms that should help you in making this counter). The counter should resent when it is not counting. Let's call the enable signal for the counter *en_repcnt* and have a signal which goes high when the count reaches 50 (500 ms) named *repcnt50*. We get the following state graph:



The state machine is intended to run at the 100 MHz clock rate. This can actually be implemented with two states, but three makes it a bit more interesting.

Simulate the design to verify the button repeat rate, then synthesize and test in the FPGA.

To turn in:

1. Report discussing what you did.
2. VHDL source (with comments) for all modules incorporated in the document.
3. Screenshot of simulation showing correct button repeat rate.
4. Design Summary showing successful synthesis.